N-Channel MOSFETs With Embedded Silicon–Carbon Source/Drain Stressors Formed Using Cluster-Carbon Implant and Excimer-Laser-Induced Solid Phase Epitaxy

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***Abstract*—In this letter, we report the use of a novel cluster-carbon ($C_7H_7^+$) implant and pulsed-excimer-laser-induced solid-phase-epitaxy technique to form embedded silicon–carbon (Si:C) source/drain (S/D) stressors. A substitutional carbon concentration $C_{\rm sub}$ of ∼1.1% was obtained in this letter. N-channel MOSFETs (n-FETs) integrated with embedded silicon–carbon (Si:C) S/D stressors formed using the novel cluster-carbon implant and pulsed-laser-anneal technique demonstrate improvement in current drive of 14% over control n-FETs formed with Si preamorphization implant. $I_{\rm OFF}-I_{\rm DSAT}$ comparison shows a 15% $I_{\rm DSAT}$ enhancement for n-FETs with embedded Si:C S/D at an $I_{\rm OFF}=1$ nA/μm despite a slightly higher series resistance.**

***Index Terms*—Laser anneal, molecular carbon, silicon carbon, solid phase epitaxy (SPE), strain.**

I. Introduction

MOBILITY-ENHANCEMENT techniques are needed to sustain continued improvement in CMOS performance. Silicon–carbon (Si:C) source/drain (S/D) stressors have been demonstrated to induce tensile strain in n-channel MOSFETs (n-FETs) for electron-mobility and drive-current ($I_{\rm DSAT}$ or $I_{\rm ON}$) enhancement [1]–[9]. While it is straightforward to integrate embedded Si:C S/D in bulk [2], [3] and silicon-on-insulator [4], [8] transistors using an S/D recess etch and selective epitaxy process, integration of S/D stressors is generally more challenging in ultrathin-body [5] or multiple-gate [6], [7] device architectures due to lack of physical margin for S/D recess etch. An attractive and simple approach to form Si:C S/D using implantation of carbon ions (C^+) and solid phase epitaxy (SPE) was recently demonstrated [9], which also has potential for adoption in advanced device architectures. As compared to C^+ implant, implantation of cluster-carbon or cluster-C or ClusterCarbon can achieve higher throughput. There are however no reports on use of molecular- or cluster-C implant for forming Si:C S/D in devices, although Si:C has been successfully formed with cluster-C implant and anneal [10], [11]. Laser anneal on cluster-carbon-implanted S/D has also not been explored.

In this letter, we report the first demonstration of n-FETs with Si:C S/D formed using a novel cluster-carbon implant and pulsed-laser-induced SPE. Cluster-C implant amorphizes the Si surface, eliminates the Ge preamorphization implant, enables precise control of junction depth, and simultaneously introduces a high dose of C at high throughput. The pulsed-laser anneal (PLA) achieves laser-induced SPE of Si:C and also high dopant activation well above their maximum solid-solubility limit [12]–[14]. Strained n-FETs with Si:C S/D having a substitutional carbon concentration ($C_{\rm sub}$) of 1.1% were fabricated, showing 15% drive-current enhancement over control devices.

II. Device Fabrication

As starting substrates, 8-in p-type bulk wafers were used. After defining the active regions, well implant, threshold voltage V_t adjust implant, and antipunchthrough implant were performed. Poly-Si/SiO_2 gate stack, S/D extension, and silicon nitride SiN spacers were formed. Implantation of cluster-carbon ($C_7H_7^+$)(8×10^{15} cm^{-2}) into the S/D region was performed for strained n-FET wafers; and Si implant (1×10^{15} cm^{-2}) was performed on the control n-FET wafers. The implant energies of the cluster-C implant are 2, 3, 7, and 10 keV to achieve a uniform carbon concentration in the top ∼40 nm of the carbon-containing region. A SiO_2 hardmask on the poly-Si gate blocked the $C_7H_7^+$ or Si implant. The S/D amorphization depth for all wafers were matched. In this experiment, the thickness of the carbon-implanted region was not varied. As^+ implant (8×10^{14} cm^{-2} at 25 keV) and a spike anneal were done to form deep S/D regions [Fig. 1(a)]. No apparent carbon diffusion was observed after the spike anneal, as confirmed using secondary-ion-mass-spectroscopy analysis. This was followed by a higher dose but shallower As^+ S/D implant (2×10^{15}cm^{-2} at 15 keV) to improve the contact resistance of the nonsilicided

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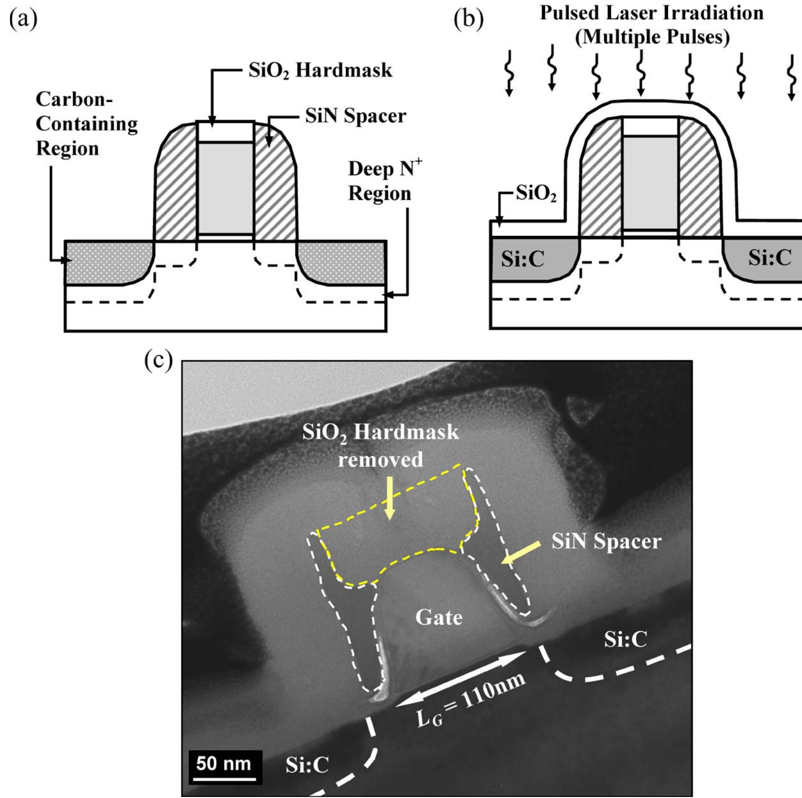

Fig. 1. Schematics illustrating the key process steps employed in this letter for fabricating n-FETs with Si:C S/D stressors. This includes cluster-carbon $(C_7H_7^+)$ and arsenic As^+ implant to form the structure in (a). A SiO_2 layer is deposited prior to pulsed-laser anneal, as shown in (b). TEM image of the n-FET having Si:C S/D with $C_{\rm sub}$ of 1.1% is shown in (c). Spacer critical dimension of the n-FETs is 30–35 nm. The sidewall profile of the polysilicon gate is tapered due an unoptimized gate etch.

S/D regions. This implant also amorphizes the Si surface as it exceeds the threshold-damage-energy density for amorphous-layer formation [15]. A 30-nm-thick SiO_2 layer was deposited to minimize carbon out-diffusion in a subsequent laser anneal. Laser annealing was carried out using a 248-nm KrF excimer laser with a pulse duration of 23 ns. The laser anneal employed multiple pulses with a fluence in the range of 350 to 710 mJ/cm^2 [Fig. 1(b)]. The amorphous Si layer absorbed the laser energy. Following laser anneal, SPE occurred in the C-containing regions to form the crystalline Si:C S/D stressors with good carbon substitutionality and dopant activation. Fig. 1(c) shows a transmission-electron-microscopy (TEM) image of an n-FET with Si:C S/D formed by $C_7H_7^+$ implant and laser anneal.

III. Results and Discussion

High-resolution X-ray diffraction (HRXRD) was used to obtain $C_{\rm sub}$ in $C_7H_7^+$-implanted and laser-annealed samples. Fig. 2 shows the HRXRD spectra of various $C_7H_7^+$-implanted Si samples after five pulses of laser irradiation. The laser fluence was varied. The laser-energy threshold for the melting of Si is 520 mJ/cm^2 [18]. As a higher $C_{\rm sub}$ of $\sim$1.1% was obtained at an energy fluence of 350 mJ/cm^2, which is in the nonmelt regime, this condition was employed in device integration. The use of nonmelt laser anneal in device fabrication avoided integration challenges such as melting of the gate associated with the use of high laser fluence [19]. This PLA condition was employed in device integration to ascertain the effects of the

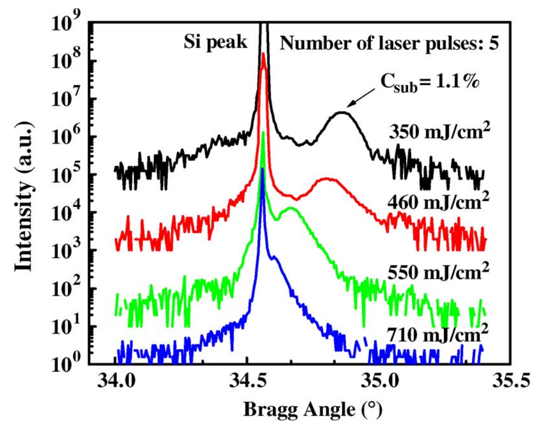

Fig. 2. HRXRD spectra of $C_7H_7^+$-implanted Si samples irradiated with five laser pulses. The laser anneal employed multiple pulses with a fluence ranging from nonmelt regime to melt regime was performed on the blanket wafers to explore the effect of multiple-laser irradiation on the carbon substitutionality in Si. Substitutional carbon concentration ($C_{\rm sub}$ or y) of 1.1% was obtained at 350 mJ/cm^2. The Si:C grown on Si is under tensile strain, and its lattice constant perpendicular to the Si surface is $a^{\perp}_{{\rm Si}_{1-y}C_y}(y) = [a^{\rm relaxed}_{{\rm Si}_{1-y}C_y}(y) - a^{II}] \times [1 + 2(C_{12}(y)/C_{11}(y))] + a^{II}]$, where $a^{\rm relaxed}_{{\rm Si}_{1-y}C_y}(y)$ is the relaxed lattice parameter of Si:C, a^{II} is the in-plane lattice constant of Si, and $C_{11}(y)$ and $C_{12}(y)$ are the elastic constants of Si:C. The value of $a^{\rm relaxed}_{{\rm Si}_{1-y}C_y}(y)$ and thus $C_{\rm sub}$ can thus be obtained [16], [17].

Si:C S/D formed by the novel $C_7H_7^+$ implant and laser-induced SPE on electrical performance.

Fig. 3 shows the $I_{\rm DS}$–$V_{\rm GS}$ and $I_{\rm DS}$–$V_{\rm DS}$ characteristics of strained n-FET with Si:C S/D and control n-FETs having a gate

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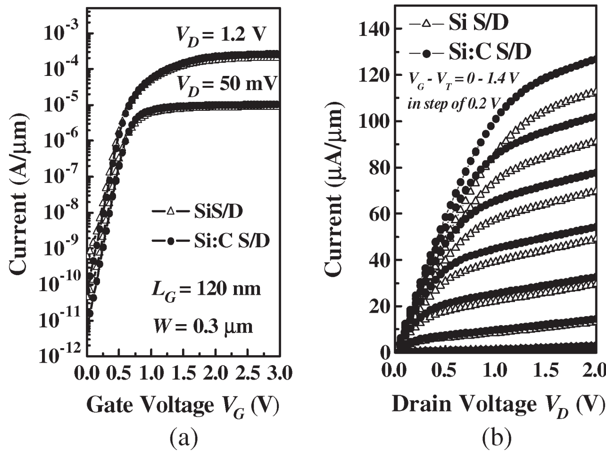

Fig. 3. (a) I_{DS}–V_{GS} characteristics of n-FETs showing comparable DIBL and subthreshold swing. (b) N-FET with Si:C S/D shows 14% drive-current enhancement over control n-FET.

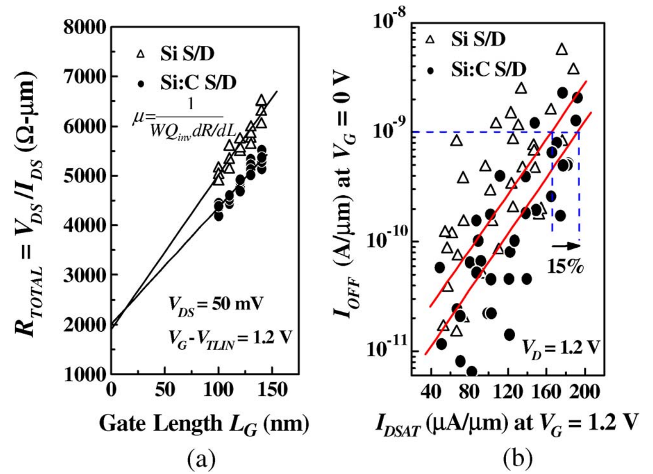

Fig. 4. (a) Total resistance $R_{\mathrm{TOTAL}}(= V_{\mathrm{DS}}/I_{\mathrm{DS}})$ as a function of gate length. Devices with Si:C S/D have a smaller slope dR_{TOTAL}/dL_G, indicating enhanced mobility. Series resistance is slightly higher in n-FETs with Si:C S/D. (b) I_{OFF}–I_{DSAT} plot obtained from a large number of devices shows that at a fixed I_{OFF} of 1 nA/μm, n-FETs with Si:C S/D has an I_{DSAT} enhancement of 15% over control devices.

length L_G of 120 nm. Drain-induced barrier lowering (DIBL) and subthreshold swing for both devices are closely matched. The OFF-state current I_{OFF} is slightly lower for the n-FET with Si:C S/D. This could be due to reduced defect densities [20] at the interface between amorphous and crystalline regions for cluster-C-implanted device, as compared to the control device which was implanted with Si. The I_{DS}–V_{DS} plot shows a 14% drive-current enhancement for the n-FET with Si:C S/D over the control n-FET at a gate overdrive (V_{GS}–V_T) of 1.2 V. This enhancement is attributed to tensile strain induced in the channel by the Si:C S/D stressors. The drain–current values reported here is lower as compared to state-of-the-art devices due to the large EOT (3 nm) used and nonsilicided S/D regions.

Direct measurement of localized strain is a major metrological challenge, and TEM-based methods usually disturb the strain during TEM sample preparation. Next, a total resistance slope-based approach [21], [22] was employed to investigate the carrier-mobility enhancement in short-channel devices. Fig. 4(a) shows the total resistance $R_{\mathrm{TOTAL}}(= V_{\mathrm{DS}}/I_{\mathrm{DS}})$ as a function of gate length L_G for both n-FETs with Si:C S/D and control n-FETs. The slope dR_{TOTAL}/dL_G is lower for n-FETs with Si:C S/D, which indicates mobility enhancement due to strain contributions from the Si:C S/D stressors. The series resistance R_{SD} for n-FETs with Si:C S/D, however, is slightly higher than the control n-FET. This is attributed to reduced dopant activation in Si:C S/D as compared to Si S/D. Despite this, drive current is still higher for the n-FETs with Si:C S/D. An even higher drive-current enhancement can be achieved if the R_{SD} issue can be resolved. In Fig. 4(b), we compare the $I_{\mathrm{OFF}}-I_{\mathrm{DSAT}}$ characteristics. More than 30 n-FETs with L_G ranging from 100 to 140 nm were characterized for each device split. An $\sim$15% I_{DSAT} enhancement for n-FETs with Si:C S/D at an I_{OFF} of 1 nA/μm was observed. Further work is needed to explore the impact of varying the Si:C thickness and to compare cluster-C and C^+ implants, for a given C_{sub} or carbon-concentration profile. Further investigation to explore manufacturability would require integration of this technique in a full CMOS process flow.

IV. Conclusion

We have demonstrated the first integration of a novel Cluster-Carbon $\mathrm{C_7H_7^+}$ implant and pulsed-excimer-laser-induced SPE technique to form Si:C S/D stressors in n-FETs. A substitutional carbon concentration of 1.1% was obtained. n-FETs with Si:C S/D show a drive-current enhancement of $\sim$14% over control n-FETs and is attributed to strain-induced effects. Cluster-carbon implant and anneal is a simple and attractive technique to integrate lattice-mismatched S/D stressors in devices and could be considered for possible adoption in future technology generations.

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