

RTP Activation

The different implant series then had been annealed in a Levitor™ 4200 for SPER temperatures between 600°C and 800°C in N₂ or He, both as spike anneals and soak anneals with soak times between 0 and 2min. The usage of that tool allowed the application of very high ramp-up rates. Three different ramp rates had been used ranging from an average of 38K/sec to 600K/s, determined between 550°C and 650°C respectively. In line with [07], the regrowth of B doped <100> material should be completed by 650°C, even at ramp rates used in this work. Some wafers have seen an additional post-anneal at 950°C (spike anneal) after the regrowth to investigate deactivation effects. Additionally, different wafers with the same implants had been spike annealed in He ambient in between 950°C and 1075°C (peak width in the range of 1.5sec) to cover the entire temperature range and to benchmark with other authors.

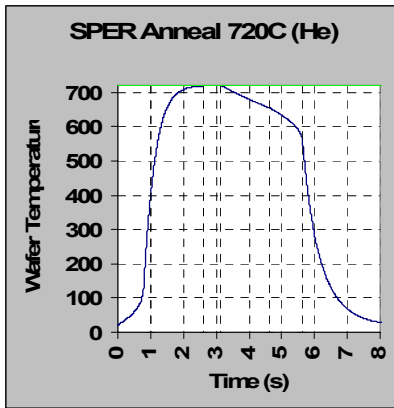


Figure 2: Fast ramp annealing profile for 720°C

Metrology

SIMS probes proved the repeatability of the B₁₈H_x. The chemical profile as implanted intersects with the 5E18cm⁻³ doping level at around 13nm. Due to the constant implant range and a correlated constant amorphization depth, simple sheet resistance measurements were used as a representative measurement of the activation level for the as implanted chemical doping profile. Some four-point-probe measurements were double checked with contact less RsL sheet resistance measurements.

3. Results

Effect of Peak Temperature during SPER

The SPER experiments confirmed that the activation increases with the peak temperature. While other authors reported a typical 50% increase of R_s [01, 04], for ¹¹B⁺ within a Ge PAI and subsequently soak anneal in the temperature regime between 800°C and

900°C, the B₁₈H_x cluster implant together with a fast ramp He-spike anneal does not show any significant reverse annealing behavior. The R_s value for all those samples decreased monotonously with temperature.

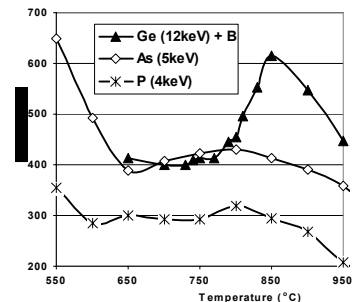


Fig 3: ¹¹B⁺ into deep PAI and slow ramp anneal (source [1])

Any pre-anneal at lower than the 950°C anneal (600-800°C) caused the sheet resistance to increase indicating a worsening of either the activation rate or the carrier mobility.

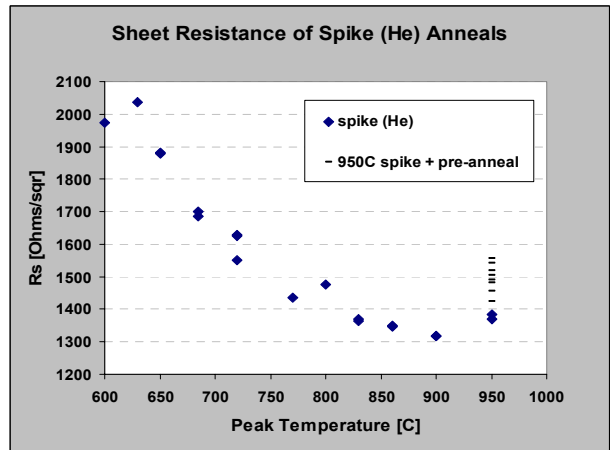


Figure 4: No reverse annealing effect can be seen. Junction depths, measured by SIMS were 12.7nm for <700°C, 13nm for 720°C and 15.5nm for 950°C.

Ramp Rate Effects

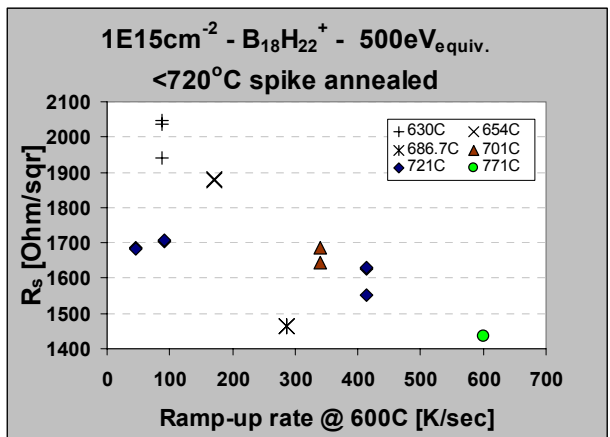


Figure 5: Besides the maximum temperature, ramp-up rate effects help to boost conductance

Ramp rate effects as reported in various publications could be confirmed. The values for the highest ramp-up rates coincided with the highest ramp-down rates by tool design. They resulted in the lowest sheet resistance. Even though the results suggest that besides the ramp rate, more parameters affected sheet resistance, the general trend is clearly seen for SDE anneals.

Soak time effects

The soak time had a minor effect, except the 720°C spike anneal. A small trend can be seen to increase the R_s with increasing times (see fig 6). For comparison reasons, a 950°C spike anneal using the same ramp rates is displayed in fig. 6. Comparing the different almost diffusion-less 720°C anneals that had been subsequently annealed a second time with a 950°C spike anneal, the sheet resistance was found to decrease by a few percent, more so for shorter anneals. In part this might be due to the diffusion ($x_j = 13\text{nm}$ for 720°C and $x_j = 15.7\text{nm}$ for 950°C). Mobility and deactivation effects need to be considered in parallel. However, the values by far did not decrease to the value obtained by the 950°C spike anneal without any pre-anneal. In the scope of this investigation it was not determined whether the mobility degraded or the Boron was deactivating during the pre-anneals.

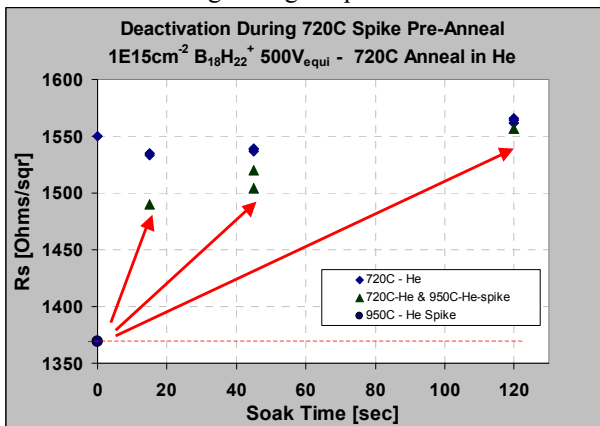


Figure 6: Activation as a function of soak time at 720°C and R_s degradation during subsequent spike anneal at 950°C. The circle at 1369Ω/sqr indicates the R_s of a 950°C anneal without pre-anneal and the arrows indicate the conductivity loss due to the pre-anneals.

Halo Activation

Using a 5keV equivalent $B_{18}H_x$ implant at doses from $1E13$ to $1E14\text{cm}^{-2}$, the R_s had been measured after a 720°C spike anneal or a 720°C soak anneal of 45sec soak time. The results are shown in Fig 7 and demon-

strate reasonable activation.

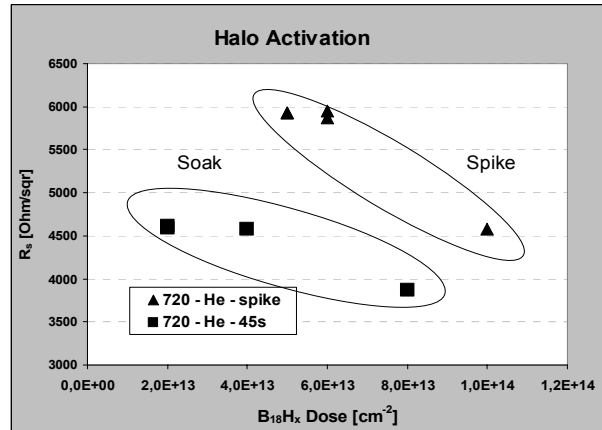
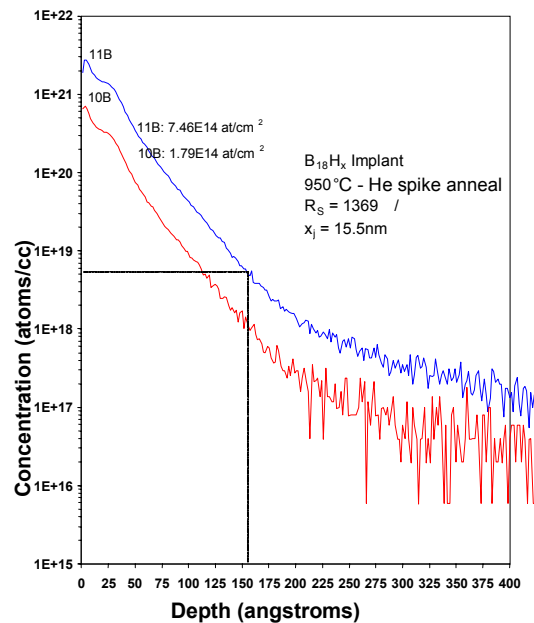


Figure 7: B - Halo activation during SPER

Annealing at 720°C to 950°C

As seen in Fig 3, the temperature regime from 720°C up to 950°C can be investigated posing an interesting compromise between minimal diffusion and SPER-type activation levels for SDE anneals. Fig. 7 demonstrates an example of a single 950°C spike anneal of a $B_{18}H_x$ implant.



At any temperature an additional Ge PAI did increase the sheet resistance considerably while the junction depth only decreased marginally. SPER with BF_2^+ implanted wafers had even higher sheet resistances than monomer boron or cluster boron implants likely due to incomplete regrowth for the chosen spike profiles.

3. Conclusions and Summary

The combination of self amorphizing B₁₈H₂₂ implants and high ramp rate spike SPER anneals look as a valid option in an advanced CMOS planar integration scheme if NFET halos are also done with the same technology. The obvious reduction of interstitials might have a beneficial effect of not only transient enhance diffusion, but also on the deactivation mechanism.

The absence of reverse annealing effects in the temperature regime beyond 800°C allows the use of even higher SPER temperatures, optimizing the regime in the R_s-x_j area. At 950°C, junction depths of less than 15.7nm are achieved, measured at 5E18cm⁻³. The sheet resistance is at around 1370Ω/□ for boron implant conditions, matching 500eV and 1E15cm⁻² without any co-implants.

As a explanation for not having the reverse annealing effect we suggest taking into account (1) a much smaller number of remaining interstitials during the SPE anneal beyond the a-Si/c-Si interface. We also take into account (2) that the time to form extended defects and B-I clusters from interstitials (plus-one-model) might not be enough during the fast ramp.

Carbon as used in conjunction with ¹¹B⁺/PAI looks attractive to further push the activation levels.

Acknowledgments

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References

- [1]. R. Lindsay, S. Severi, B. J. Pawlak K. Henson, A. Lauwers, X. Pages, A. Satta, R. Surdeanu, H. Lenzian, and K. Maex , SPER junction optimisation in 45nm CMOS devices *IWJT 2004*
- [2]. B. J. Pawlak, W. Vandervorst, et al, Enhanced boron activation in silicon by high ramp-up rate solid phase epitaxial regrowth, *APL* **86**, (12), 2005,
- [3]. S. Severi, K.G. Anil et al, Diffusion-less junctions and super halo profiles for PMOS transistors, *IEDM 2004*
- [4]. W. Lerch, S. Paul et al, Solid Phase Epitaxy, Activation and Deactivation in USJ,
- [5]. D. Jacobson, Using Boron Cluster Ion Implantation to Fabricate Ultra Shallow Junctions, *5th International Workshop on Junction Technology 2005*
- [6]. Nariaki Hamamoto et al., Decaborane implantation with the medium current implanter, *IIT 2004*
- [7]. T.W. Gibbons, J.F. Sigmon, Solid Phase Regrowth, in J.M. Poate, J.W. Mayer, *Laser Annealing of Semiconductors*, p325